Evaluating the Influence of Standard Cell Libraries in two Circuit Reliability Estimation Methods

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***Abstract*—Methods to estimate circuit reliability are important, especially when nanometer technologies are involved. In this context, the methods PTM (Probabilistic Transfer Matrices) and SPR (Signal Probability Reliability) are explored in this paper. The reliability of different versions of circuits that implement the same logic function is investigated. The evaluation compared the results between the different circuits and between the different estimation methods. This work shows a significant reliability difference for equivalent circuits.**

***Index Terms*—Reliability, PTM, SPR, Standard-Cell**

I. Introduction

Logic circuits are getting in nanometric scale. This makes them more sensitive to faults, resulting in new challenges to designers in this area [1]. Most of nanometer circuit are designed using the standard cell logic flow. This flow is generally composed by three synthesis steps: "High-level synthesis", "Logic synthesis" and "Physical synthesis" [2]. The logic synthesis receive a "Register-transfer level description" and using a standard cell library, provides a "Multi-level logic circuit". The used library has a direct influence in the final circuit version [3].

This work will explore circuits described in "Multi-level logic". In this description it is possible to verify the logic influence in circuit reliability. Also, two methods were selected that estimate the reliability of a logic circuit. The first is Probabilistic Transfer Matrices or PTM. It is an exact method and requires a lot of memory resources. The second is Signal Probability Reliability or SPR. It is a fast method which introduces some deviation in the reliability metric when in the presence of a fanout.

Thus, the first objective of this work is to explore the reliability of different versions of circuits that implement the same logical function. The second objective is to analyze and verify a possible relation between the reliability values obtained by PTM and SPR methods.

This work is organized as follow: Section II presents an overview of estimation methods used to compute logic circuit reliabilities. In Section III, the methodology is presented. All results are shown and discussed in Section IV. Finally, the conclusion is presented in Section V.

II. Reliability Analysis

Many methods that estimate the reliability of a circuit have been proposed. However, the Probabilistic Transfer Matrices (PTM) framework, proposed by Patel et al [4], is one of the most credible [5]. This is a method that obtains an accurate reliability result from a logic circuit. The major disadvantage of the method is the amount of information to be generated by the circuits. In contrast, there is the Signal Probability Reliability (SPR) method, which compared to the computational cost of PTM, is extremely fast. However, the presence of reconvergent fanouts compromise the final reliability result [6].

A. Probabilistic Transfer Matrices

PTM is a precise method to estimate the reliability of a circuit. This accuracy is due to the fact that PTM represents, through matrices, all the possibilities of input and output of a circuit. The method was extensively explored by Krishnaswamy et al [7]. The main idea of PTM is to correlate the inputs and outputs of a circuit, based on its topology and individual reliability of each logic gate. For this purpose, matrices representing the logic gates are used. As shown in the Fig. 1, the matrix is constructed from the truth table Fig. 1(a). There is two types of matrices in method, PTM matrix 1(c) that represents the behavior of the gate or circuit in the presence of faults, and ITM (Ideal Transfer Matrix) matrix 1(b) that represents the fault free gate.

Input	Input	Output
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

(a)

$$\begin{array}{c|cc} & \mathbf{0} & \mathbf{1} \\ \mathbf{00} & 1 & 0 \\ \mathbf{01} & 1 & 0 \\ \mathbf{10} & 1 & 0 \\ \mathbf{11} & 0 & 1 \end{array}$$

(b)

$$\begin{array}{c|cc} & \mathbf{0} & \mathbf{1} \\ \mathbf{00} & q & 1-q \\ \mathbf{01} & q & 1-q \\ \mathbf{10} & q & 1-q \\ \mathbf{11} & 1-q & q \end{array}$$

(c)

Fig. 1: AND's gate (a)Truth Table, (b)ITM and (c)PTM

The operations used in the method are the multiplication of matrices and the application of the Kronecker tensor. The difference between the two matrices operations is the dimension of product matrix. In a two matrix multiplication with their respective dimensions $(m \times n)$ and $(o \times p)$, the product matrix it will has the dimension $(m \times p)$. In the

Kronecker product of the same two matrices, the final matrix dimension will be $((m * o) \times (n * p))$.

In the Figure 2 are shown how, from a circuit, the PTM matrix of the entire circuit is formed. At this point, it is already possible to verify one of the main problems of the PTM: the exponential growth of the sizes of the matrices.

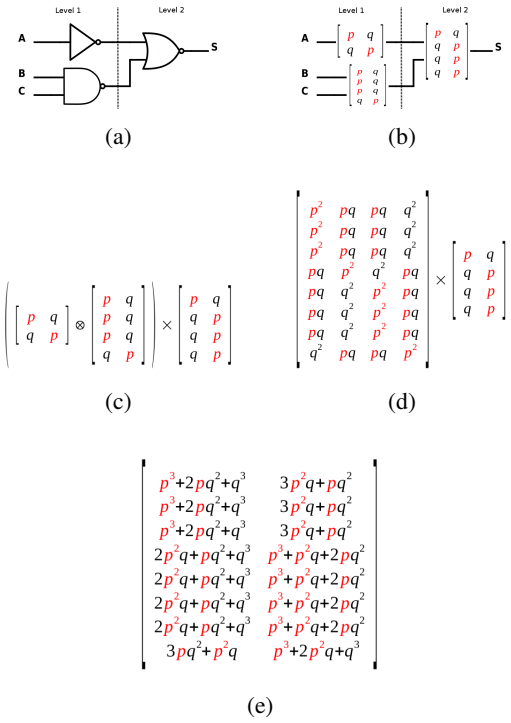

Fig. 2: Steps to obtain the whole circuit's PTM matrix: (a)Circuit in levels, (b)PTM gates' matrices, (c)PTM method, (d)Kronecker's tensor and (e)Matrix multiplication

The reliability value is extracted from the relation between the PTM and ITM matrices of the entire circuit. The result will be the sum of all the elements of the PTM matrix that correspond to elements "1" of the ITM matrix. The equation to obtain the reliability of the whole circuit is demonstrated in the Equation 1. If the probabilities of the input signals of the circuit are considered fault-free, and present probability of 50% to be logic 1 and 50% to be logic 0, Equation 2 is more suitable. The PTM method is an accurate method of estimating the reliability of a circuit, but the required computational cost makes it impracticable to be used for large circuits, even with techniques that improve the efficiency of the method [8].

$$R_c = \sum_{ITM_c(i,j)=1} p(j|i)p(i) \tag{1}$$

$$R_c = \frac{1}{2^n} \sum_{ITM_c(i,j)=1} p(j|i) \tag{2}$$

B. Signal Probability Reliability

Obtaining the reliability value of a circuit is also possible by probabilities of the signals [9]. Such an approach suggests that the occurrence of a correct output can be determined by the cumulative computation of the effects of multiple faults from the input signals of the circuit. It takes into account all the interactions of the signals and their prone to faults until the circuit output signals. A matrix is formed to demonstrate the 4 possible states of a signal: 0-correct (0c), 1-correct (1c), 0-incorrect (0i) and 1-incorrect (1i). Thus, each signal's matrix is calculated from input to output circuit order.

In Figure 3, the sequence of steps to obtain the signal matrix of the output of an AND logic gate is shown. As it is possible to observe in the sequence of steps, the operations between the signals and the logic gates, taking into account the parallel and serial positioning, is identical to the PTM method. Nevertheless, according to the Figures 3(b) and 3(c), the PTM and ITM matrices of the ports are used to compute the matrices of the output signals.

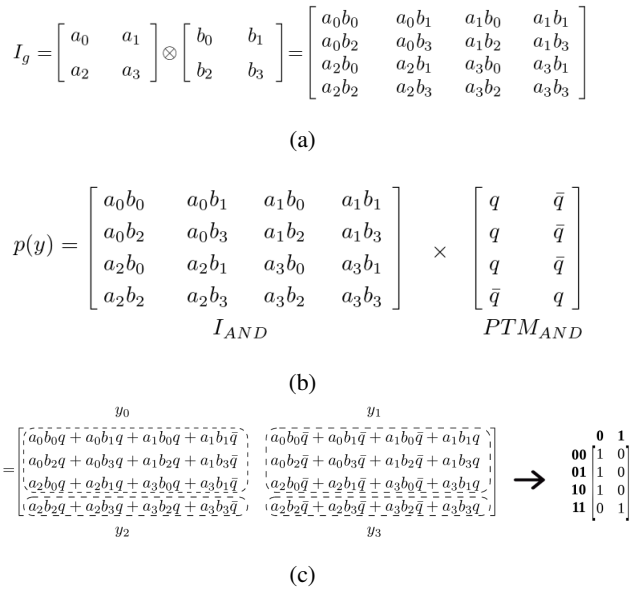

Fig. 3: Steps to apply SPR method in a gate: (a)Input Computation, (b)PTM's Gate Combine, (c)ITM relation with Gate Matrix

After traversing the entire circuit, the reliability value of the method will be extracted from the probabilities of the output signals. As shown in the equation 3, where R_j corresponds to the reliability of the j^{th} output . Comparing computational performance, the SPR method has a linear complexity to the number of logic gates in the circuit. However, the accuracy is directly related to the presence of fanouts. This is because when a signal is divided into fanout, the same signal is computed at the same time in different ways, propagating a null value, which generates differences in the final result of reliability.

$$R_c = \prod_{j=0}^{m-1} R_j \tag{3}$$

III. Methodology

In this Section we present the methodology used to achieve our goal. Due to the memory limitation of PTM method, we used the small circuits presented in [10]. The logic function implemented by each circuits are shown in Equations 4 to 7. The rest of this section is divided in two topics, one related to the logic synthesis process and the second to the reliability computation.

$$\begin{aligned} C8Output \\ 1 &= !C * !B \\ 2 &= !(C + B) + A \\ 3 &= (B + C) * !D \end{aligned} \tag{4}$$

$$C9Output = !C + !(!D * !C) + !(!C + B + A) \tag{5}$$

$$C10Output = H + !G + !F + (!(D * C) * !(!E * (!B + !A))) \tag{6}$$

$$\begin{aligned} C11Output &= W1 * W2 \\ W1 &= !(C * B * A * ((!G * F) + (G * !F)) \\ W2 &= !H * (!E + !D)) * I \end{aligned} \tag{7}$$

A. Circuit Technology Mapping and Analysis

The sample utilized was composed of four different circuits, each mapped to three different libraries, therefore generating twelve mapped Verilog files for analysis. Regarding the used libraries, they were named "XY-Z" (based on the amount of different gates in each library), being X the maximum number of NMOS transistors in series and Y the maximum number of PMOS transistors in series. The Z value reflects the maximum number of series/parallel associations. As the number of allowed transistors rises, so do the number of distinct complex gates. This increases memory usage and CPU time in both technology mapping and reliability computation, but lowers the area and delay of the mapped circuit and increases its reliability, as partly seen in [3].

The benchmark set was mapped using the ABC Sequential Synthesis and Verification tool [11]. The circuits were then subsequently exported to technology-independent Verilog files to be used with custom tools created for circuit analysis and reliability. Technology Mapping was also used for possible logic optimization/simplification, consequently lowering the number of fan-outs and increasing circuit reliability.

The circuit analysis tool was a Python program that read all Verilog files in a folder and output gate and level data in table form so it could be used to easily generate statistic and probabilistic data for further comparisons of the circuit reliability results.

B. Circuit Reliability Computation

All of the twelve Verilog files were then run in a Java program to receive both PTM and SPR reliability values. The tool required a mapped Verilog file and a library file that contains all the gate types used in the mapped circuit for it to properly compute the reliability.

Another detail of the tool was selecting the data type to be used in the PTM method so it could properly compute the reliability of the circuit and not result in inaccurate values or memory errors. Supported types were float(32-bit precision), double(64-bit precision) and BigDecimal (Java class that represents exact numbers instead of floating-point).

After all the required inputs and the circuit reliability method were selected, the tool required a gate reliability value for it to calculate and return the reliability of the circuit. The gate reliability value utilized was 0.99.

After the data were collected, tables were made to: compare PTM and SPR methods and compare the reliability values of different mapped versions of a circuit. These comparisons were created with the purpose of finding a correlation or tendency of the SPR values while comparing them to the PTM values, and thus deduce whether or not the SPR method could be used to identify the reliability behavior of a circuit.

IV. Results

To study the correlation between the SPR and PTM methods, the effect of standard-cell libraries and compare the reliability values for different versions of the same logic function, the data were grouped by PTM and SPR values, number of gates, number of levels and number of fan-outs, generating 2 tables for analysis. Table II provide the number, for each circuit, of: gates, which are the elements in the circuit most susceptible to faults, levels, since they propagate the faults from previous gates in the circuit to other gates, and fan-out occurrences, which is the primary factor for the unpredictability of the SPR method. We can infer that, due the reasons depicted previously, as number of gates and levels decreases, the circuit reliability increases. However, the same cannot be said for the number of fan-outs, since it does not follow a pattern.

Table I, on the other hand, contains circuit reliability values (PTM and SPR) and the difference in percentage between the two; these computations were made for all twelve mapped circuits. The technology mapping process reduces the number of gates and levels which in turn increases the overall reliability of the circuit; on the other hand, the mapping does not take fan-out minimization or optimization into account, thus generating more variation in the final reliability for SPR values.

The rest of this section is divided in two parts, one compares the reliability values between the 3 mapped verilogs of a circuit and the other compares the PTM method with the SPR method while analyzing the data obtained as a whole.

TABLE I: Circuit Reliability Values. The gate reliability value used was 0.99.

Circuits	**C8**			**C9**			**C10**			**C11**		
Library	**22-1**	**33-1**	**33-2**	**22-1**	**33-1**	**33-2**	**22-1**	**33-1**	**33-2**	**22-1**	**33-1**	**33-2**
PTM	0,9242	0,9407	0,9412	0,9734	0,9864	0,9863	0,9783	0,9783	0,9798	0,9615	0,9707	0,9758
SPR	0,9200	0,9380	0,9373	0,9642	0,9839	0,9857	0,9783	0,9783	0,9798	0,9642	0,9719	0,9768
(PTM-SPR)%	-0,46%	-0,29%	-0,42%	-0,94%	-0,25%	-0,06%	0,00%	0,00%	0,00%	0,28%	0,13%	0,11%

TABLE II: Circuit Information

Circuit	**#GATES**	**#LEVELS**	**#FANOUTS**
C8-22-1	13	4	5
C8-33-1	12	3	6
C8-33-2	9	3	5
C9-22-1	11	4	3
C9-33-1	5	3	1
C9-33-2	3	3	2
C10-22-1	8	4	0
C10-33-1	8	4	0
C10-33-2	7	2	0
C11-22-1	16	4	3
C11-33-1	14	4	3
C11-33-2	9	3	3

A. Reliability Analysis for Different Versions of a Circuit

From the values shown on Table I it is evident that the SPR method is not a foolproof way to define which, of a group of circuits with the same logic function, is more reliable, since the circuit with the most reliability is different between the two methods (the circuit mapped with library 33-2 for the PTM method and the circuit mapped with library 33-1 for SPR). The table also presents the number of gates for each version of C8, supporting the fact that the lower the number of gates, the higher the reliability.

The two different versions of C10 are a special case where the circuit has no fan-outs; consequently, the SPR and PTM values are the same, since SPR's unpredictable behavior only happens when there's at least one fan-out. The different versions for C9 and C11 show the expected behaviour for when the number of gates and levels drop.

B. Reliability Analysis for the PTM and SPR Methods

Excluding C10, which has no fan-outs, C11 is the only circuit where the SPR method could correctly define the most reliable version of the circuit. For C8 the most reliable circuit is the one mapped by library 33-2 (C8_33-2), while the highest SPR value obtained was from library 33-1 (C8_33-1). The same happens for C9, being the most reliable circuit C9_33-1 and the SPR method obtaining C9_33-2 as the most reliable one. Also, while the different versions of C8 and C9 display a higher PTM value than the corresponding SPR values, C11 reveals that SPR values being lower than the PTM values is not always the case.

Furthermore, the data on the table indicate that as number of logic gates in a standard cell library rises, so does the circuit reliability.

V. Conclusion

Given the difference between the obtained circuit reliability results, it can be concluded that the robustness of a circuit changes in relation to the types of gates used to compound the structure. And there is no direct relation in reliability values obtained by PTM and SPR methods. Because, for C8 and C9, the SPR method underestimated the circuit reliability compared with the PTM, while for C11 it overestimated. In future works the influence of fanouts position in circuit structure can be explored in SPR method, since C9 e C11 are similar but, using PTM as base, they have different reliability behavior; computational cost, such as CPU time and number of operations, could also be considered, in order to highlight the accuracy and performance of both methods.

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